Abstract of the Disclosure

Disclosed is an apparatus for controlling a bank refresh including 2^N of banks, comprising: N input buffer for buffering N bank address signals inputted from an external circuit with the command signal, a (N-1)-nary counter which is reset by an output signals from the N input buffer, a switch for combining count signals from the (N-1)-nary counter in order to produce internal bank refresh signals in response to external bank address signals from the N buffer and a chipset controller for generating a plurality of internal bank addresses for the refresh using the internal bank refresh signals.